REMARKS

As noted previously, the Applicant appreciates the Examiner's thorough examination of the subject application.

Claims 1-18 and 21are pending in the application and were rejected in the non-final Office Action mailed 05 December 2008 on various statutory grounds, as described in further detail below. Claims 1, 18, and 21 are amended herein. No new matter has been added. Applicant <u>requests reconsideration</u> and further examination of the subject application in light of the following remarks.

Claim Objections

Concerning item 2 of the Office Action, the Examiner objected to the term "substantially equal" in what the Examiner identified as claim 20. Applicant believes the Examiner meant to indicate claim 21 as claim 20 had been previously canceled. In response to the objection, the term "substantially equal" has been deleted from claim 21.

Claim Rejections – 35 U.S.C. § 102

Concerning items 3-6 of the Office Action, claims 18 and 21 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,922,065 to Hull et al. ("Hull"). Applicant respectfully traverses the rejection and requests reconsideration for the following reasons.

For a rejection under 35 U.S.C. § 102(b) to be proper, the cited reference must teach, either expressly or inherently, each and every limitation of the claim(s) at issue. In this situation, Hull fails to teach (or suggest) each and every limitation as arranged in claims 18 and 21. Applicant therefore submits that the rejection is improper and should be withdrawn accordingly.

Independent claim 18 has been amended to recite "*(i) instruction packets comprising a plurality of only control instructions, <u>the control instructions having a control bit width,</u> and (ii) instruction packets comprising a plurality of instructions comprising at least one data processing*

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instruction, the data processing instructions having a data processing bit width wider than the control bit width,". Claim 1 is amended is similar fashion. This amendment is supported by at least page 7, line 29 to page 8, line 11 and FIG. 2 of the subject application as filed.

In addition, independent claim 21 has been amended to recite *"instruction packets including a first type of instruction packet comprising a plurality of only control instructions of equal width, the control instructions having a control bit width, and a second type of instruction packet comprising a plurality of instructions comprising at least one data processing instruction, the at least one data processing instructions having a data processing bit width wider than the control bit width,"*. This amendment is supported by at least page 7, line 29 to page 8, line 11 and FIG. 2 of the subject application as filed.

The Applicant submits that the amended claims are novel over Hull because Hull does not disclose, at least, *"control instructions having a control bit width, and ... data processing instructions having a data processing bit width wider than the control bit width"*. Hull, column 3, lines 61 to 63, recites that *"all instructions in the instruction set of the processor are 41 bits in length"*. Therefore, Hull explicitly discloses that all the instructions have the same bit width (41 bits).

Thus, for at least the foregoing reasons, Hull fails to teach (or suggest) all of the limitations of independent claims 18 and 21 of the subject application. Hull therefore forms an improper basis for a rejection of claims 18 and 21 under 35 U.S.C. § 102(b), and Applicant requests that the rejection of these claims be removed accordingly.

Claim Rejections – 35 U.S.C. § 103

Claims 1-7, 11 and 14-17

Concerning items 7-20 of the Office Action, claims 1-7, 11, and 14-17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hull, cited previously, in view of "Unifying FPGAs and SIMD Arrays" by Bolotski et al. ("Bolotski"). Applicant traverses the rejection and requests

reconsideration for the following reasons.

One requirement for a claim rejection under 35 U.S.C. § 103(a) is that the cited reference(s) teach or suggest each and every limitation as recited in the claim(s) at issue. Another requirement for a rejection under 35 U.S.C. § 103(a) is that proper motivation must exist to combine or modify the teachings of the reference(s) in the way proposed by the Examiner for the rejection. As will be explained (and without acceding to the presence, propriety, or sufficiency of the motivation adduced by the Examiner), the cited references fail to teach or suggest all of the limitations of Applicant's claims 1-7, 11, and 14-17, as will be explained.

For the claimed invention of the subject application, the different types of instructions each have a different bit width. For example, amended claim 1 recites "the data processing instructions having a data processing bit width wider than the control bit width". The specification of the subject application explains that the control instructions can have a 21 bit width, the memory instructions can have a 28 bit width and the data instructions can have a 34 bit width. This disclosed at page 7, line 30 to page 8, line 9, of the subject application as filed, which recites "*Instruction packet 211 …includes three 21-bit control instructions (c21)*"; "*Instruction packet 212 includes a 34-bit data instruction (d34) and a 28-bit memory instruction (m28)*"; and "*Instruction packet 213 includes a 34-bit data instruction (d34) and a 21-bit control instruction (c21)*". These instructions packets are illustrated in FIG. 2 of the subject application as filed set out below.
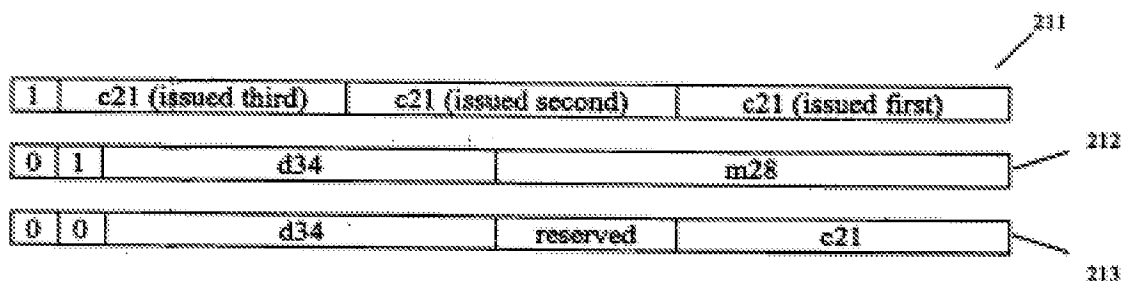
The use of different sized instructions optimizes the performance of the computer processor,

by optimizing the processing of each different type of instruction. For example, page 5, lines 19 to 23 recite that *"Typically, control code ... is difficult to parallelize, ... and its code density is generally more important than its speed performance. By contrast, datapath code typically ... is highly parallelizable, ... and its performance is more important than its code density"*. The use of different sized control and data instructions allows each type of instructions to be optimized as a result of their different, specialized functions.

Hull dose not discuss the differences between control and data instruction or discuss the need to optimize the processing of each different type of instruction. In addition, when provided with Hull, it would not have been obvious to a person skilled in the art to amend Hull such that each different type of instruction has a different width, since there is no teaching of this feature or its advantages in Hull, and Hull does not disclose how to process instructions which have different bit widths. In fact, **Hull explicitly states that the instructions have the same width (41 bits)**.

As illustrated in Hull, FIG. 4, every instruction bundle must contain three instructions. In contrast, the instructions packets of the subject application may contain different numbers of instructions depending on the type of instructions included. FIG. 2 of the subject application illustrates an instruction packet comprising three instructions (211) and instruction packets comprising two instructions (212, 213). This arrangement is possible as a result **of the different sized instructions**. Since the control instructions are shorter than the data instructions, each packet comprising only control instructions can contain more instructions than a packet containing at least one data instruction. This helps to increase the control code density.

The arrangement of the instruction packets of Applicant's claims allow for several processing arrangements. An instruction packet comprising only control instructions (such as packet 211 of FIG. 2) defines that the three control instructions must be processed sequentially in the predefined order, as can be seen from FIG. 2 of the subject application and recited in, e.g., claim 1 ("wherein, in use the decode unit causes instructions of (i) instruction packets comprising a plurality of only control instructions to be **executed sequentially** on the control processing channel").

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Hull does not teach or suggest this arrangement as recited by the Applicant. Referring to FIG. 4 of Hull an instruction bundle, such as template B contains three branch instructions. Template B does not have any double lines (42, 43) separating the instructions, consequently the three instructions of template B can be processed sequentially **in any order**. There is no order defined by Hull for processing the three branch instructions. The double lines (42, 43) function as stop-bits, indicating, for example in template 1, that slot0 and slot1 must be processed before slot2. The control instructions of Applicant's claims are processed in the specific sequential order (in effect the instruction comprises two stop bits). This arrangement is not disclosed or even hinted at in Hull and there is no teaching in Hull of generating instruction bundles having three sequential instructions.

For Applicant's claimed invention, the different types of instruction packets define the type of processing which can be performed. Instruction packets of type 211 (only control) must process the three instructions sequentially in a specific order, and instruction packets of type 213 (only data) and of type 212 (data, and data or control) must process the two instructions simultaneously. Simultaneously processing means both instructions read their source registers before either instruction writes its destination registers. In contrast, there is no way for an instruction bundle of Hull to dictate that two instructions MUST be executed simultaneously.

As explained in Applicant's specification, the initial indicator bit of each packet indicates the instructions behavior. For example, page 8, lines 14 to 18 of the subject application recites "*as shown in Fig. 2, an initial indicator bit "1" signifies that an instruction packet is of a scalar control instruction type, with three control instructions; while initial indicator bits "0 1" and "0 0" signify instruction packets of type 212 and 213, with a data and memory instruction in packet 212 or a data and control instruction in packet 213*".

The hard distinction between one packet type (211) which mandates sequential operation and two packet types (212 and 213) which mandate simultaneous operation provides all that the machine needs for efficient execution of code, without the complexity of Hull's many templates. This is reflected in the use of 1 or 2 bits of the packet to indicate instruction behavior, rather than 5 bits for

Hull. This results in denser code and easier decoding for the machine of the subject application.

The Examiner cites Bolotski as teaching a system than can simulate SIMD and configurable operations on the same and for teaching that the advantages of combining a SIMD and a configurable unit include reducing costs. Bolotski does not cure the deficiencies noted previously for Hull relative to independent claim 1 of the subject application (the base claim for claims 3-4 and 17).

Thus, when provided with Hull (and/or Bolotski), it would not have been obvious to a person skilled in the art how to amend the processor of Hull such that the processor of the claimed invention results. Accordingly, Hull and Bolotski (whether considered alone or in combination) fail to teach or suggest each and every limitation of independent claim 1 of the subject application. For at least the foregoing reasons, the cited combination of Hull and Bolotski forms an improper basis for a rejection of claims 1-7, 11, and 14-17 under 35 U.S.C. § 103(a), and Applicant requests that the rejection be withdrawn accordingly.

Claims 8-10, 12, and 13

Concerning items 21-22 of the Office Action, claims 8-10, 12, and 13 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hull and Bolotski, cited previously, in view of the holding(s) in In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955) and/or In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976). Applicant traverses the rejection and requests reconsideration as, without acceding to the Examiner's allegations set forth for the rejection, the combination of Hull and Bolotski does not teach or suggest each and every limitation of claim 1, the base claim for claims 8-10, 12, and 13, as was explained *supra*.

For at least the foregoing reasons, the cited combination of Hull and the holding(s) in In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955) and/or In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1076) forms an improper basis for a rejection of claims 8-10, 12, and 13 under 35 U.S.C. § 103(a), and Applicant requests that the rejection be withdrawn accordingly..

Response to Arguments

Concerning item 24 of the Office Action, the Examiner stated that the claims as previously presented did not include limitations as to certain instructions being longer than other instructions. The Applicant notes that <u>independent claims 1, 18, and 21 have been amended to recite instructions of different lengths</u>. Thus, consistent with the Examiner's statement in item 24 and Applicant's arguments provided above, claims 1-18 and 21 and their dependent claims are believed to be patentable over the cited art.

Conclusion

In view of the remarks submitted herein, Applicant respectfully submits that all of the pending claims in the subject application are in condition for allowance, and respectfully requests a Notice of Allowance for the application.

Authorization is hereby given to charge deposit account, No. 50-1133, for the fees corresponding to a Petition for Extension of Time (three months) under 37 CFR § 1.136, and for any other fees that may be required for the prosecution of the subject application.

If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

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